Dramatically Accelerate 96Board Software via an FPGA with Integrated Processors

Glenn Steiner, Sr. Manager, Xilinx, Inc.

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Key Takeaways:
With the drive to increase integration, reduce system costs, accelerate performance, and enhance reliability, software developers are discovering the processor they would like to target is simply not fast enough. This session will help you the system architect or software developer understand how you can architect and develop software on an FPGA integrated processor, and accelerate software code via FPGA accelerators.

Abstract:
As a software developer, in order to meet system level performance requirements, you may have realized that your next software project will be targeting a processor inside of an FPGA. How will this impact your development process and what benefits might you gain with this tight integration of processor and FPGA? Starting from the basics of what FPGAs are (in terms of software programming), this session will provide a simple to understand primer of what modern FPGAs with embedded processors can do. We will wrap up with examples of how high level synthesis tools can move software to programmable logic hardware enabling dramatic software acceleration.
What is a Field Programmable Gate Array (FPGA)?

Why Use a Heterogeneous All Programmable MPSoC?

How Do You Program Heterogeneous All Programmable Devices?

Introducing the Xilinx Ultra96 Development Platform

Software Acceleration Design Example
- German Traffic Sign Recognition

Summary
### Complexity Continues to Increase
- Designers Need Better Ways to Architect, Design &

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<td>▪ Cloud-RAN</td>
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<td>▪ Industry 4.0</td>
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<td>▪ Embedded Vision</td>
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<td>▪ Cyber-Physical</td>
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Performance & Power Scalability

System Integration & Intelligence

Security, Safety & Reliability
What is a Field Programmable Gate Array (FPGA)?
A field-programmable gate array (FPGA) is an integrated circuit designed to be configured by the customer or designer after manufacturing—hence “field-programmable” —Wikipedia

In their simplest form FPGAs contain:
- Configurable Logic Blocks
  - AND, OR, Invert & many other logic functions
- Configurable interconnect
  - Enabling Logic Blocks to be connected together
- I/O Interfaces

With these elements an arbitrary logic design may be created
FPGAs - Circa 1990

- Glue Logic
- Simple State Machines
- Prototyping

Logic that could be connected quickly
- Like LEGO blocks
What Today’s FPGAs Can Do

- Prototyping or Glue Logic
- System Integration (SoC)
- Connectivity – Bridging, Switching
- Digital Signal Processing (DSP)
- Contain Complete Embedded Processing Systems
- Accelerate Software

Chips that can do any Intelligent Function - Like LEGO Mindstorms Blocks
Why Use a Heterogeneous All Programmable MPSoC?
All Programmable Heterogeneous Processing Diversity – The Right Processing Element for the

- Application Processors – High performance general computing

- Graphics Processing Unit – Graphical User Interface

- Real-time Processors – Low latency deterministic operation
  - Lock step for reliable operation

- Platform Management Unit Processor
  - Triple redundant for system management & error handling

- Configuration & Security Unit Processor
  - Triple redundant for reliable configuration & security operation

- Programmable Logic – Software acceleration, additional or custom peripherals
The Heterogeneous All Programmable Advantage

**Technical**
- Performance
- Power
- Flexibility

**Business**
- Time to Market
- Lower Cost
- Flexibility

**Highest Level of System Integration and Intelligence**

The Right Engines for the Right Task
Why Heterogeneous Processors?

- **Non-Critical Tasks**
  - Linux
  - General Purpose Processor

- **Critical Tasks**
  - Motor Control (Real-Time Response)

**Network Interface**

**INTERRUPT**

**Compute-Intensive Non-Critical Tasks**

**On-Chip Memory**

**Tightly-Coupled Memory**

**Real-Time Processing**

**RTOS**
Today’s “FPGAs” → Heterogeneous All Programmable Devices

**CG Devices**
- Dual-Core A53s

**EG Devices**
- Quad-Core A53s
  - GPU

**EV Devices**
- Quad-Core A53s
  - GPU and Video Codec

- **High Speed Peripherals**
  - PCIe Gen2, USB 3.0, DisplayPort

- **FPGA Acceleration**
  - 16nm UltraScale+ Fabric
  - Customizable Engines

- **Configuration & Security Unit**
  - Anti-Tamper & Trust Industry Standards

- **Platform & Power Management**
  - Granular Power Control
  - Functional Safety

- **Memory Subsystem**
  - DDR3/4
  - LPDDR3/4

- **Memory Subsystem**
  - 16G & 33G Transceivers
  - PCIe® Gen4

- **Platform Management Unit**
  - 100G Ethernet
  - 150G Interlaken

- **Config and Security**
  - ARM Mali™-400MP2

- **System Functions**

- **DisplayPort**
- **USB 3.0**
- **SATA**
- **PCIe® Gen2**
- **GigE**
- **CAN**
- **SPI**
- **SD/eMMC**
- **NAND**

- **ARM Cortex-A53**
  - ARM Mali™-400MP2
  - System Functions

- **ARM Cortex® R5**
  - GPU

- **Graphics Processor**
  - ARM Mali-400MP2
  - 2D/3D Visualization

- **Video Codec**
  - 8K4K (15fps)
  - 4K2K (60fps)

- **Application Processors**
  - 64-bit ARMv8
  - Up to 1.5GHz

- **Real-Time Processors**
  - 32-bit Dual-Core
  - Up to 600MHz

- **ZU11EG, ZU15EG, ZU19EG Only**
- **100G Ethernet**
- **150G Interlaken**

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Flexibility - All Programmable Devices Accelerate Development & Enable Change Management

- Rapidly Implement & Test designs
- Accommodate Late Breaking Design Changes
- In System Field Upgradability
- Build Next Generation with New Capabilities
  - Use same Board & Chipset w/ reprogrammed devices
- Dynamic Partial Reconfiguration
  - Re-program FPGA regions during operation
- HW – SW Co-debug
  - Implement Logic Analyzers inside FPGAs for better visibility into hardware-software problems
How Do You Program Heterogeneous All Programmable Devices?
Software Development Flow

- Create Software Platform and Project
- Download and Test Software Design
- Debug Software Application
- Profile Software Application for Performance
Software Development Kit

- Eclipse based IDE
- Windows and Linux hosted
- GUI and command line interface
- Everything you need for
  - Board bring-up
  - Firmware development
  - Bare-metal application development
  - Linux application development
  - Performance optimization
  - System deployment
### Run Time Software

Begin Application Development with Validated OS’s
Determine the Right Processor for your Application

#### OS Ecosystem

<table>
<thead>
<tr>
<th>OS</th>
<th>Hypervisor Support</th>
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<tbody>
<tr>
<td>Linux: Mentor, Wind River</td>
<td>APU: No, RPU: No, Micro-Blaze: Yes</td>
</tr>
<tr>
<td>Xen Hypervisor</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
</tr>
<tr>
<td>Android</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
</tr>
<tr>
<td>Bare metal</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
</tr>
<tr>
<td>eSol eT-kernel</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
</tr>
<tr>
<td>FreeRTOS</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
</tr>
<tr>
<td>GreenHills – INTEGRITY</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
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<tr>
<td>LynxOS7, LynxSecure</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
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<tr>
<td>Mentor Hypervisor, Nucleus</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
</tr>
<tr>
<td>Micrium - uC/OS-II &amp; III</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
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<tr>
<td>QNX</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
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<tr>
<td>Sciopta</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
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<tr>
<td>Sysgo – PikeOS</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
</tr>
<tr>
<td>Wind River VxWorks7/Rocket</td>
<td>APU: Yes, RPU: Yes, Micro-Blaze: Yes</td>
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</tbody>
</table>

#### High-Level OSs
- Stand-alone Drivers & Libraries

#### Open Source / No Fee
- Safety Certifiable
- Cross-Processor OS Support
- Commercial
Introducing the Xilinx Ultra96 Development Platform
Ultra96 Features

- Linaro 96Boards Consumer Edition
  - 85mm x 54mm form factor
- Zynq UltraScale+ MPSoC ZU3EG
- 2GB LPDDR4 Memory
- MicroSD Socket
- WiFi
- Ports
  - Mini DisplayPort
  - 2x USB 3.0 Type A downstream ports (Host)
  - 1x USB 3.0 Micro-B upstream port (Device)
  - 40-pin Low-speed expansion header
  - 60-pin High speed expansion header
Mezzanine Cards

» Compatible with 96Boards Mezzanine Boards

» Grove 96Boards Sensor Mezzanine (board or bundle)
  - 9 Grove connectors for 96Boards IO
    5x GPIO, and 4x I2C (mixed 3.3V and 5V; all 5V tolerant)
  - 9 Grove connectors for ATMEGA328 IO
    5x GPIO, 3x ADC, and 1x I2C (all 5V)
  - 2 6-pin SPI headers
  - MicroUSB interface to 96Boards console serial port
  - 1 Power LED & 3 user LEDs
  - Power & Reset buttons

» Grove Starter Kit (Includes Mezzanine Board)
  - LCD, Relay, Buzzer, LEDs, Sound Sensor, Touch Sensor, Light Sensor, ...
Ultra96 SD Card Image

- Linux Kernel v4.9
  - Supports Ultra96 peripherals
  - MALI 400 GPU support
  - Enlightenment Desktop

- Easy-to-use web interface
  - Access via WiFi or monitor, mouse, keyboard

- Run Example Projects for Grove devices
- Edit, compile and run demo applications
- Add custom content
- Access Tutorials

Ultra96 SD Card Image
Accelerating Software via Programmable Logic
Now I Can Turn Software into Hardware

- Profile Your Code
- Identify Time Consuming Functions
- Automatically Create & Attach Hardware Accelerators
- Model & Optimize for Performance
- Download & Run
Acceleration Examples

- MRI Back Projection Algorithm 8x
- 16k FFT 10x
- Optical Flow 25x
- Stereo Local Block Matching 25x
- 2D Video Optical Filter 30x
- Binary Neural Network 8,600x
Software Acceleration Design Example
German Traffic Sign Recognition
Neural Network Example

- German Road Sign Database
  - 50,000+ 32x32 bit images for training
  - 44 classes (43 road signs, 1 background)
  - Training via Amazon Web Services
    - AWS: p2.xlarge Instance – 8 hours $7.78 6.5e

- Binary Neural Network Characteristics
  - 6 convolutional layers
  - 2 max pool layers
  - 3 fully connected layers
Neural Network Performance Results

Up to 8,600 times faster when accelerated with programmable logic

<table>
<thead>
<tr>
<th>Performance Metric</th>
<th>Software Only</th>
<th>Programmable Logic Accelerated</th>
</tr>
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<tbody>
<tr>
<td>Tiles per second</td>
<td>2.2</td>
<td>19,000</td>
</tr>
<tr>
<td>Scene rate (fps)</td>
<td>0.011 (92 sec per frame)</td>
<td>94</td>
</tr>
<tr>
<td>Overall Acceleration</td>
<td>-</td>
<td>8,600X</td>
</tr>
</tbody>
</table>
## Accelerated Image Classification

### Realtime Metrics

**Tiles per Second**

incl. DMA: 19156  
BNN only: 20416.4

Tiles per second in Software: 2.17

Images per second in Hardware: 94.8317

Acceleration factor (HW/SW): 8827.65

<table>
<thead>
<tr>
<th>Speed</th>
<th>Percentage</th>
<th>Description</th>
<th>Percentage</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>30 Km/h</td>
<td>91%</td>
<td>Priority crossroad</td>
<td>64%</td>
<td>20 Km/h</td>
</tr>
<tr>
<td>80 Km/h</td>
<td>3%</td>
<td>Give way</td>
<td>22%</td>
<td>No overtaking</td>
</tr>
<tr>
<td>Road slippery when wet or dirty</td>
<td>2%</td>
<td>Bend to right</td>
<td>5%</td>
<td>120 Km/h</td>
</tr>
<tr>
<td>Bicycles crossing ahead</td>
<td>1%</td>
<td>Risk of snow or ice</td>
<td>4%</td>
<td>Bicycles crossing ahead</td>
</tr>
<tr>
<td>Road works</td>
<td>1%</td>
<td>Road slippery when wet or dirty</td>
<td>3%</td>
<td>Stop</td>
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Go Faster with Development Platforms

- Leverage Proven Content
- Rapid Prototyping
- Reduced Time to Market
- Reduced System Level Costs

Your “Stuff”
Reference Designs
OS / Hypervisor
Software Development
Development Kits
Silicon

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The Future is *Ultra96* Contest

➤ Submit your most creative, most out-of-the-box AI or ML application at the Xilinx or Avnet table during Demo Friday (12:00 – 16:00)

➤ The best **25** get a **FREE Ultra96 board** plus software to help you realize their vision

➤ Submit a working design within 60 days and get a T-shirt and SWAG. It’s that simple.

➤ Winner announced through Xilinx social media channels. If it’s you, you’re invited to present your design to your peers in industry at Xilinx Developer Forum 2018
Summary:
No Need to Fear Your Processor Being Inside an FPGA

- Industry Standard Development Environments
  - Develop, Compile, Link & Download
  - Easy On-Chip Debugging including HW-SW Co-Debug

- Extensive IP Libraries, Drivers & Popular OSs

- Automated Tools for Creating SW Accelerators

- Pre-Built Reference Designs Enable Quick-Starts
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February 2018

Questions?
96Boards Sensors Kit

96Boards Sensors Mezzanine Card
- Integrated ATMEGA328p microcontroller (Arduino compatible)
- 18 Grove connectors
- Arduino UNO compatible shield connectors
- UART interface between baseboard and microcontroller
- USB-UART connector for baseboard console and control

Grove Sensors
- LCD RGB Backlight
- Smart Relay
- Buzzer
- Sound Sensor
- Touch Sensor
- Rotary Angle Sensor
- Temperature & Humidity Sensor
- LED
- Light Sensor
- Button
- LEDs Blue, Green, Red
- Mini Servo
- Grove Cables